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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,972	02/25/2004	Richard P. Schubert	A0312.70519US00	4114

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EXAMINER	
SONG, JASMINE	
ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,972	SCHUBERT, RICHARD P.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 22-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. The drawings filed on 02/25/2004 have been approved by the Examiner.

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 06/21/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Election/Restrictions

5. Applicant's election without traverse of elected Group I in the reply filed on 12/11/2006 is acknowledged. The traversal is on the grounds that the claims in Group I and II are sufficiently related that there would be negligible burden on the Examiner from considering the claims in Group II in conjunction with the claims in Group I. This is not found persuasive because each subcombination has utility other than in the disclosed combination, i.e., Group I is directed to enable at least one sense amp associated with a line in the way when the information indicates an item is store in the way without having a control circuit outputting a plurality of timing signals with a first timing signal coupled to the timing input of the data array and a second timing signal connected to the enable input of the sense amp. Furthermore, Group II is directed to time signals, which is required to searched class 713. note each group is distinct from each other and examination of the entire application would cause serious burden to examiner since search and examination of Group I does not require to search class 713. Thus, the restriction requirement is proper.

The requirement is still deemed proper and is therefore made FINAL.

6. This application contains claims 10-21 drawn to an invention nonelected with traverse. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-9 and 22-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Osada et al., US 6,091,629.

Regarding claim 1, Osada teaches a method of operating a cache in a computer system, the cache storing items associated with addresses in memory in the computer system, the cache having at least one way with a tag array and a data array (Fig.8), with information in the tag array indicating, for each address applied to the cache, whether information in the data array is associated with the applied address in memory (Fig.8 and col.9, lines 42-52), with the data array implemented as an array of cells connected to lines and a plurality of sense amps, with a sense amp being connectable to each of the lines (Fig.6), comprising, for each of the at least one way:

a) making a determination, based on information stored in the tag array, whether an item associated with the applied address is stored in the way in the data array (col.9, lines 42-53);

b) altering the state of at least one line in the way associated with the applied address starting before completing the determination (it is taught as writing data in a data array before establishment of a hit signal, col.2, lines 23-29 and col.10, lines 4-5);

c) after completing the determination, when the information indicates an item is stored in the way in the data array (it is taught as the hit signal is a hit, col.10, lines 5-8), enabling at least one sense amp associated with a line in the way when it is determined that an item associated with the applied address is stored in the way (col.6, lines 50-53).

Regarding claim 2, Osada teaches each sense amp is connectable to a plurality of lines and enabling the sense amp associated with a line in the indicated way comprises connecting the sense amp to a single one of the plurality of lines selectively in response to the information read from the tag array (Fig.6, col.7, lines 48-61).

Regarding claim 3, Osada teaches additionally comprising providing as a bit in the output of the cache, the output of the sense amp (Fig.1, it is taught as switches).

Regarding claim 4, Osada teaches the data array is implemented as memory having a plurality of banks, with each applied address associated with one or more lines in one of the banks and not associated with lines in at least a portion of the plurality of banks, the method further comprising, between the time that an address is applied to the tag array and an output is provided from the sense amp, performing a memory operation in a bank in the portion of the plurality of banks (Fig.6, col.7, lines 48-64).

Regarding claim 5, Osada teaches the at least one way comprises 2 ways (2 ways cache memory is well know in the CAM, it can be considered as two banks in the

Fig.6 of Osada, please also see applicant's specification page 4).

Regarding claim 6, Osada teaches the at least one way consists of 4 ways (4 ways cache memory is well know in the CAM, please also see applicant's specification page 5 says that a cache can have any number of ways).

Regarding claim 7, Osada teaches making a determination comprises for each way in the cache: reading a tag field from a location in the tag array and comparing the value in the tag field to a portion of the bits in the applied address (Fig.8).

Regarding claim 8, Osada teaches additionally comprising controlling the charge on each of the plurality of lines in the data array to place the lines in a predetermined state before starting to alter the state of the line (it is taught as place lines in a low signal at the time of writing data, col.6, lines 13-14).

Regarding claim 9, Osada teaches each of the lines comprises a column line in the memory and altering the state of at least one line comprises asserting a word line in the memory (Fig.1).

Regarding claim 22, Osada teaches a method of operating a cache in a computer system, the cache storing items associated with addresses in memory in the computer system, the cache having a tag array and a data array (Fig.8), the data array

having a plurality of ways with information in the tag array indicating, for each address applied to the cache, in which, if any, way in the data array information associated with the applied address is stored (Fig.8 and col.9, lines 42-52), with the data array implemented as arrays of cells connected to lines and plurality of sense amps, with a sense amp being connectable to each of the word lines (Fig.6),

a) applying a first portion of the applied address to the tag array to address a location in each way of the tag array (Fig.8, col.9, lines 42-44);

b) comparing a second portion of the applied address to information read from the addressed locations in each way of the tag array to produce at a first time, an indication of a match between the first input and one of the ways (col.9, lines 42-53);

c) before the first time, altering the state of lines associated with the first portion of the applied address in each way of the data array, with the state of the lines based on information stored in the data array (it is taught as writing data in a data array before establishment of a hit signal, col.2, lines 23-29 and col.10, lines 4-5); and

d) after the first time, sensing the state of a line associated with the first portion of the applied address in the data array, with the sensed line selected (col.6, lines 50-53) in response to the output of the comparator(it is taught as the hit signal is a hit, col.10, lines 5-8).

Regarding claim 23, Osada teaches each of the lines comprises a bit line in a semiconductor memory (Fig.1).

Regarding claim 24, Osada teaches altering the state of lines comprises activating a cell connected to a word line in the semiconductor memory (col.8, lines 11-13).

Regarding claim 25, Osada teaches additionally comprising placing the lines in a predetermined charge state (col.8, lines 11-15).

Regarding claim 26, Osada teaches altering the state of the lines comprises altering the charge on each line based on information stored in one memory cell (col.8, lines 11-25).

Regarding claim 27, Osada teaches each of the lines comprises a differential pair and altering the charge on the line comprises altering the charge difference between the lines(col.8, lines 11-25).

Regarding claim 28, Osada teaches sensing the state of a line comprises enabling a sense amp selected based on the indication of a match (col.6, lines 50-53)

Regarding claim 29, Osada teaches sensing the state of a line comprises activating a multiplexer based on the indication of a match to connect a selected line to a sense amp (Fig.6 and Fig.8).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jasmine Song

Patent Examiner

March 5, 2007